Vel Tech Multi Tech Dr.Rangarajan Dr.Sakunthala Engineering College

(An Autonomous Institution affiliated to Anna University)

Department of Electronics and Communication Engineering

PG M.E VLSI Design

Regulation 2019

Syllabus

Academic Year 2019-20

Category	Foundation Course			
Course code	192MA101			
Course Title	**Graph Theory andOptimization Techniques**			
Semester –I	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	4	0	0	4

Unit-1	**BASIC CONCEPTS IN GRAPH THEORY**	**12**

Common families of graphs, degree sequence, handshaking lemma, Havel-Hakimi theorem (statement only). Walk, trail and path, connected graph, distance, radius and diameter. Graph isomorphism. Representations of graphs - adjacency and Incidence lists - adjacency and incidence mantes. Digraph - orientation. strongly, weakly and unilaterally connected digraphs

Unit-2	**GRAPH ALGORITHMS**	**12**

Trees, spanning trees, matrix tree theorem. Search algorithms - depth first search and breadth first search. spanning tree algorithm -Kruskal's and Prim's, shortest path algorithm

Unit-3	**APPLICATION OF GRAPH ALGORITHMS**	**12**

Dijkstra's flow networks: flows and cuts in networks, solution of the maximum flow problem - characterization of maximum flow Maxflow MM-cut Theorem (statement only), algorithms - maximum flow, augmenting path, and FFEK - maximum flow.

Unit-4	**LINEAR PROGRAMMING**	**12**

Formulation, simplex method, two phase method, simplex multipliers, dual and primal, dual simplex method. Transportation model - initial basic feasible solution- north-west corner rule, (east cost method, Vogel's approximation method, and optimum solution of transportation problem.

Unit-5	**DYNAMIC PROGRAMMING**	**12**

Principle of optimality, backward and forward recursion, calculus method of solution, tabular method of solution, shortest-route problem, Knapsack model.

References

1	West D B, Introduction to graph Theory, Pearson Education. New Delhi, 2018.
2	Hamdy A Taha, Operations Research: An Introduction, Pearson Education. New Delhi, 2017.
3	NarasinghDeo, Graph Theory: with applications to engineering and computer science, PHI Learning, 2017.
4	Kambo N.S., Mathematical Programming Techniques. East - West Press, New Delhi. 2012
5	Jonathan L Gross and Jay Yellen, Graph Theory and its Applications, Chapman 8 Hall, New York, 2006.

Category	Programme core			
Course code	192VL121			
Course Title	**MOS DEVICE PHYSICS**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**MOS CAPACITORS**	9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

Unit-2	**MOSFET DEVICES**	9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

Unit-3	**CMOS DEVICE DESIGN**	9

MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements

Unit-4	**CMOS PERFORMANCE FACTORS**	9

Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source–Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS

Unit-5	**BIPOLAR DEVICES**	9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal I_C–V_{CE} Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on

Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between BV_{CEO} and BV_{CBO}.	
References	
1	BehzadRazavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition.
2	J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer 2002 Edition.
3	Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition.

Category	Programme core			
Course code	192VL122			
Course Title	**Digital IC Design**			
Semester –I	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	3	0	0	**3**

Unit-1	**OVERVIEW OF VLSI DESIGN METHODOLOGY**	**9**
VLSI design process Architectural design Logical design, Physical design- Layout styles - Full custom. Semicustom approaches. Layout design rules: Need for design rules - Layer representations - CMOS N-Well / P-Well design rules - Design rule backgrounder-Layer assignments SOI rules.		
Unit-2	**MOS INVERTER:**	**9**
Static characteristics Resistive load inverter - Inverter with n-type MOSFET load CMOS inverter - Transient characteristics Delay time definitions, calculation of delay times, power analysis .		
Unit-3	**STATIC LOGIC DESIGN**	**9**
Static CMOS Design Complementary CMOS, Ratioed logic, Pass transistor and transmission gate Dynamic CMOS logic - . CMOS logic - Recharged domino logic.- Static Sequential circuits - Bistatbility, CMOS static FF		
Unit-4	**DYNAMIC LOGIC DESIGN**	**9**
Dynamic sequential circuits -Pseudo static latch. Dynamic two phase FF, Clocked- CMOS latch, NORA CMOS logic. TSPCL logic.		
Unit-5	**VLSI BUILDING BLOCKS DESIGN**	**9**
Adders, Shifters, Arithmetic logic unit design Multipliers-Array, Carry Save multiplier. Wallace tree, Booth's algorithm, Modified Booths Algorithm. Designing Memory and Array Structures-Memory peripheral circuit.		

References

1	Jan M. Rabaey,AnanthaChandrakasan, BorivojeNikolic, 'Digital Integrated Circuits, Pearson Education India, second edition, 2016.
2	Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis and Design, Fourth Edition, Tata McGraw-Hill,2014
3	Neil H.E. Weste, David Harris. 'CMOS VLSI Design: A circuits and systems perspective'Pearson, 4th edition 2015.
4	Douglas A Pucknell Kamran Eshraghian,'Basic VLSI Design. PHI learning, New Delhi. 2011.
5	Saida M Sait and youssef, 'VLSI Physical Design Automation: Theory and Practice, World Scientific Publishing Company, 1999.

Category	Programme core			
Course code	192VL123			
Course Title	**Designing with FPGAs**			
Semester –I	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**Introduction to FPGA**	**9**
XILINX 3000 series FPGAs, XILINX 4000 series FPGAs, Designing with FPGAs, Designing with FPGAs using One Hot Assignment, Altera CPLDs, Altera FLEX 10K series CPLDs.		
Unit-2	**Digital Logic Design using VHDL**	**9**
Variables, Signals, Constants, Arrays, VHDL Operators, Functions, Procedures, Packages, Libraries VHDL description of Combinational Networks, Modeling flip flops using VHDL Processes, VHDL Models Combinational Networks, Compilation and Simulation of VHDL Code, VHDL Models Sequential Machine.		
Unit-3	**Testing**	**9**
Testing Combinational Logic, Testing Sequential Logic, Scan Testing, Boundary Scan, BIST.		
Unit-4	**Synthesis of Combinational and Sequential Logic**	**9**
Introduction to Synthesis,Combinational Logic,Sequential Logic, threestate devices and bus interface, Sequential with flip flops, explicit state machine, Registered logic, state encoding,Implicit state machine, Registers, Counters, Resets, Gated clocks, Clock enables, Anticipating the results, Loops		
Unit-5	**ControllerandDSPDesign**	**9**
RISC SPM Processor, RISC SPM ALU, RISC SPM Controller, Static RAM memory, a simplified 486 Bus Model, interfacing memory to a micro processor Bus, UART. DSP blocks- FIR and IIR filters.		

References

1	Charles H. Roth, 'Digital system design using VHDL. Thomson, 2014
2	Michael D Clienti 'Advanced Digital Design with Verilog HDL Pearson education. 2005.
3	Morris Mano M, Charles R Kime, logic and Computer Design Fundamentals, Pearson Education, 2015.

Category	Programme core			
Course code	192VL124			
Course Title	**Low Power VLSI Design**			
Semester –I	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**POWER DISSIPATION IN CMOS**	**9**
Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design.		
Unit-2	**POWER OPTIMIZATION**	**9**
Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison		
Unit-3	**DESIGN OF LOW POWER CMOS CIRCUITS**	**9**
low voltage low power static Random access and dynamic Random access memories – low power clock – Advanced techniques – Special techniques		
Unit-4	**POWER ESTIMATION**	**9**
Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.		
Unit-5	**SOFTWARE DESIGN FOR LOW POWER**	**9**
Sources of software power dissipation, software power estimation, software power optimizations, codesign for low power		

References

1	Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998
2	Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
3	Kiat-send Yeo, Kaushik Roy “Low-Voltage, Low-power VLSI Subsystem”, Tata McGraw-Hill, 2009
4	AbdelatifBelaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
5	A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
6	DimitriosSoudris, C.Pignet, Costas Goutis,“Designing CMOS Circuits for Low Power”Kluwer, 2002.
7	James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.
8	J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.

Category	Programme core			
Course code	192VL125			
Course Title	**Analog VLSI Circuits**			
Semester –II	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	4	0	0	4

Unit-1	**ANALOG CIRCUIT BUILDING BLOCKS**	**12**
Switches. Active resistors. Current sources and sinks. Current mirrors. voltage references. Comparator. Multiplier. Single stage amplifiers - Common source, Common drain and common gate.		
Unit-2	**DIFFERENTIAL AMPLIFIERS**	**12**
MOS inverting amplifier - Improving performance of inverting amplifier , CMOS differential amplifiers - Qualitative and Quantitative Analysis, Characterization of Op-Amp , CMOS two stage op-amp, single stage amplifier, common mode feedback network,Gilbert cell.		
Unit-3	**LAYOUT AND PACKAGING**	**12**
CMOS design rules –antenna effect, analog layout techniques –Multi finger transistor , Symmetry – reference distribution, passive devices- interconnects- substrate coupling		
Unit-4	**DATACONVERTER FUNDAMENTALS**	**12**
Ideal A/D and D/A converters, Quantization noise, Signed codes, Performance limitations. D/A AND A/D CONVERTERS:D/A converter : Current scaling, Voltage scaling and Charge scaling D/A converters -Serial D/A converters Serial A/D converters. Parallel - A/D converters		
Unit-5	**PHASE LOCKED LOOPS**	**12**
Op-amps with output stage, Folded Cascode op-amp, Transconductance Amplifier-Noise and Distortion in Amplifiers.-Phase Detector-Voltage Controlled Oscillator-Loop Filter.		

References

1	Phillip Allen and Douglas Holberg. 'CMOS Analog Circuit Design, Oxford University Press, 2012.
2	Jacob Baker, -CMOS, Circuit Design Layout and Simulation', Wiley- IEEE Press, 2011.
3	BehzadRazavi ,DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS, McGraw-Hill,2002
4	Randall L Geiger, Phillip E Allen and Noel R Sootier, 'VLSI Design Techniques for Analog and Digital Circuits'. McGraw HA International Edition, 2010.
5	David A Johns and Ken Martin, 'Analog Integrated Circuit Design', John Wiley and Sons, 2008.
6	BenhardRazavi, 'Data Converters', Kluwer Publishers, 2005.
7	Paul R Gray and Robert G Meyer 'Analysis and Design of Analog Integrated Circuits, John Wiley and Son, 2005

Category	Programme core			
Course code	192VL12A			
Course Title	**VLSI Design Laboratory**			
Semester –I	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	0	0	4	2

1	Study of MOS and Inverter characteristics
2	Design of static and dynamic digital circuits
3	Design of Memories with Peripherals
4	Model parameter extraction for diode, BJT, MOSFET
5	Layout generation from schematics

Category	**Mandatory Course**			
Course code	192HS10A			
Course Title	**ENGLISH FOR RESEARCH PAPER WRITING**			
Semester –I	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	0	0	**	Grade

1	Planning and preparation, word order, breaking up of long sentences, structuring paragraphs and sentences, being concise and removing redundancy, avoiding ambiguity and vagueness, clarifying who did what, highlighting the findings, hedging and criticising, paraphrasing and plagiarism. (15)
2	Sections of a paper - Abstract, introduction, review of the literature, methods, results and discussions, conclusions, acknowledgements, references and the final check. (10)
3	Key skills needed to write title, abstract, introduction, review of the literature, methods, results and discussions, and conclusions of a research paper. (20)
4	Use of appropriate phrases to ensure the research paper is as good as it could possibly be the first- time submission. (15)
REFERENCES	
1	Adrian Wallwork, “English for Writing Research Papers”, Springer New York Dordrecht Heidelberg London, 2011.
2	Goldbort R., “Writing for Science”, Yale University Press, 2006.
3	Day R., “How to Write and Publish a Scientific Paper”, Cambridge University Press, 2006
4	Highman N., “Handbook of Writing for the Mathematical Sciences”, SIAM, Highman’s Book, 1998.

SEMESTER II

Category	Programme core			
Course code	192VL221			
Course Title	**VLSI Testing**			
Semester –II	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**Faults in Logic Circuits**	**9**
Stuck-at Fault, Bridging Faults, Delay Fault, Breaks,Stuck-on and Stuck-Open Faults, Controllability and Observability, Undetectable Faults, Equivalent Faults, Temporary Faults.		
Unit-2	**Fault Detection in Logic Circuits.**	**9**
Truth Table and Fault Matrix, Path Sensitization, D-Algorithm, PODEM, FAN, Delay Fault Detection, Designing Checking Experiments, Test Generation Using the Circuit Structure and the State Table.		
Unit-3	**Design For Testability**	**9**
Ad Hoc Techniques, Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Clocked Hazard-Free Latches, Double-Latch and Single-Latch LSSD, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Crosscheck, Boundary Scan.		
Unit-4	**Built-in Self-Test**	**9**
Exhaustive Testing, Pseudoexhaustive Pattern Generation, Pseudorandom Pattern Generator, Deterministic Testing, Test Pattern Generation for BIST, Transition Count, Syndrome Checking, Signature Analysis		
Unit-5	**Fault Diagnosis**	**9**
Logical Level Diagnosis, basic concepts, FaultDictionary, Guided Probe Testing, Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits. Expert systems for Diagnosis, effect cause analysis.		

References

1	P.K. Lala, "An Introduction to Logic Circuit Testing", Morgan and Claypool Publishers, 2008.
2	M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", JaicoPublishing House, 2002.
3	M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory andMixedSignal VLSI Circuits", Kluwer Academic Publishers, 2002.
4	A.L.Crouch, "Design Test for Digital IC"s and Embedded Core Systems", Prentice HallInternational, 2002.

Category	Programme core			
Course code	192VL222			
Course Title	**Computer Aided Design for VLSI Systems**			
Semester –II	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**ALGORITHM**	**9**
VLSI Design cycle - Role of CAD tools in the VLSI Design process data structures and algorithms: Complexity of algorithms, dynamic programming, Integer linear programming, Genetic algorithm.		
Unit-2	**SYNTHESIS**	**9**
Simulated Annealing. Logic synthesis - two level synthesis. Binary decision diagrams, and ROBDD principles		
Unit-3	**PHYSICAL DESIGN AUTOMATION**	**9**
Partitioning - KL, FM algorithms, Placement - Simulation based algorithms - Simulated Annealing , Force Directed Algorithm. Partitioning based algorithms- Breuer's Algorithm. Terminal propagation Algorithm Cluster Growth Algorithm Floor planning - slicing floor plan Constraint Based Floor Planning. Integer Program Based Floor Planning -Pin Assignment		
Unit-4	**ROUTING**	**9**
Grid routing - Maze Rowing Algorithms. Global routing, Shortest Path Based Algorithms, Steiner tree based Algorithms, detailed routing - Left Edge algorithm. Dog-Leg Algorithm , Greedy Channel Routing, Switch Box Routing algorithms- over the cell routing, Clock Routing		
Unit-5	**LAYOUT SYNTHESIS AND OPTIMIZATION**	**9**
Layout generation and Optimization of standard cell layout, gate matrix layout and PLA Layout Compaction - one dimensional and two dimensional compaction		

References

1	Sabih H Gerez, 'Algorithms for VLSI Design Automation John Wiley & Sons. 2008.
2	NaveedSherwani, Algorithms for VLSI Physical Design Automation, 3/e,Kluwer Academic, 2012
3	Sait S M and Youssef H. 'VLSI Physical Design Automation World Scientific, 2004.
4	Michell G D, 'Synthesis and Optimization of Digital Circuits. Tata McGraw Hill, 2003

Category	Programme core			
Course code	192VL223			
Course Title	**Hardware Verification Techniques**			
Semester –II	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	4	0	0	4

Unit-1	VERIFICATION TECHNOLOGIES	12
Importance of Verification - Reconvergence Model The Human Factor Formal and Functional Verification Approaches Timing Verification Testing Versus Verification Design and Verification Reuse - Linting -Simulation		
Unit-2	**TOOLS**	**12**
Third Party Models Verification Intellectual Property - Waveform Viewers Code Coverage Functional Coverage-Issue Tracking - Metrics - Role of the Verification Plan - Levels of Verification - Verification strategies		
Unit-3	**HIGH-LEVEL MODELING**	**12**
High-Level Versus RTL Thinking Structure of High-Level Code - Data Abstraction - Object-Oriented Programming - Parallel Simulation Engine - Race Conditions - Portability Issues.		
Unit-4	**TEST CASE GENERATION**	**12**
Simple Stimulus, Simple Output, Complex Stimulus,Bus-Functional Models - Response Monitors - Transaction Level Interface - Verification Harness -		
Unit-5	**ARCHITECTING TESTBENCHES**	**12**
Design Configuration- Self Checking - Test benches, Directed Stimulus, Random Stimulus, System Level Verification Harnesses - Transaction Level Models, Managing Simulations-Regression		

References

1	Janick Bergeron, 'Writing Test Benches Using System Verilog", Springer 1'st Edition, 2009.
2	Chris Spear. Greg Tumbush. 'System Verilog for Verification - A Guide to learning the Test bench Language Features' Springer 3rd edition, 2012.
3	KropfT, "Introduction to Formal Hardware Verification, Springer Verlag. 2010.
4	Mark Glasser, 'Open Verification Methodology Cookbook', Springer, 2009.
5	S. Andreas Meyer, 'Principles of Functional Verification'Newnes, 2003

Category	Programme core			
Course code	192VL22A			
Course Title	Advanced VLSI Design Laboratory			
Semester –II	Scheme and Credits			
	L	T	P	Credits
	0	0	4	2
1	Specification, Design, synthesis and layout design (floor planning, place and route, power and dock distribution. clock tree synthesis, timing analysis, power analysis, signal integrity, post-layout simulation and back annotation. GDS-II generation) of digital building block.			
2	Specification. Schematic Design, simulation. layout generation. Physical verification (LVS. DRC. RC extraction, post layout simulation, back annotation. GDS-II generation) of analog building block.			

Category	Employability Enhancement Course			
Course code	192VL25A			
Course Title	Industry Visit & Technical Seminar			
Semester –II	Scheme and Credits			
	L	T	P	Credits
	0	0	4	2
1	The student will make at least two technical presentations on current topics related to the specialization. The same will be assessed by a committee appointed by the department. The students are expected to submit a report at the end of the semester covering the various aspects of his/her presentation together with the observation in industry visits. A quiz covering the above will be held at the end of the semester.			

SEMESTER III

Category	Employability Enhancement Course			
Course code	192VL35A			
Course Title	Project Work-I			
Semester –III	Scheme and Credits			
	L	T	P	Credits
	0	0	6	3

1	Identification of a real life problem in thrust area
2	Developing a mathematical model for solving the above problem
3	Finalization of system requirements and specification
4	Proposing different solutions for the problem based on literature survey
5	Future trends in providing alternate solutions
6	Consolidated report preparation of the above

SEMESTER IV

Category	Employability Enhancement Course			
Course code	192VL45A			
Course Title	Project Work-II			
Semester –IV	Scheme and Credits			
	L	T	P	Credits
	0	0	28	14

1	Consolidated report preparation of the above
2	The project work involves the following Preparing a project :brief proposal including Problem identification A statement of system / process specifications proposed to be developed (Block Diagram/ Concept tree) List of possible solutions Including alternatives and constraints Cost benefit analysis Time line of activities
3	A report highlighting the design finalization (based on functional requirements &standards (if any))
4	A presentation Include the following Implementation phase(Hardware / Software / both) Testing and validation of the developed system Learning in the Project
5	Consolidated report preparation of the above

PROFESSIONAL ELECTIVE THEORY COURSES(Three to be opted for second semester)

Category	Professional Elective			
Course code	192VL23A			
Course Title	**MIXED SIGNAL VLSI DESIGN**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**SWITCHED CAPACITOR C FILTERS**	**9**
Universal active filter (KHN), Switched capacitor filters:Switched capacitor resistors - Integrator-amplifiers - comparators sample & hold circuits - Biquad.		
Unit-2	**CONTINUOUS TIME FILTERS**	**9**
Introduction to Gm - C filters - CMOS Transconductors using Triode transistors, active transistors –BiCMOStransconductors - MOSFET C Filters - Tuning Circuitry - Dynamic range performance - Elementary transconductor building block- First and Second order filters.		
Unit-3	**DIGITAL TO ANALOG CONVERTERS**	**9**
Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity		
Unit-4	**ANALOG TO DIGITALCONVERTERS**	**9**
Types of ADCs- Flash, two step, pipelined, successive approximation, folding ADC's. SIGMA DELTA CONVERTERS:Over sampled converters - over sampling without noise & with noise implementation imperfections first order modulator decimation filters second order modulator sigma delta DAC & ADC's. Non-idealities in the ADC.		
Unit-5	**ANALOG AND MIXED SIGNAL EXTENSIONS TO HDL**	**9**
Introduction Language design objectives, Theory of differential algebraic equations, the 1076.1 Language,Tolerance groups Conservative systems Time and the simulation cycle A/D and D/A Interaction Quiescent Point - Frequency domain modeling and examples. Analog extensions to Verilog: Introduction data types -Expressions – Signals, Analog behavior - Hierarchical Structures - Mixed signal Interaction.		

References

1	Phillip Allen and Douglas Holberg 'CMOS Analog Circuit Design', Oxford University Press, 2012.
2	Jacob Baker, CMOS, Circuit Design Layout and Simulation , Wiley- IEEE Press, 2011.
3	David A Johns and Ken Martin, 'Analog Integrated Circuit Design'. John Wiley and Sons. 2008.
4	BenhardRazavi, 'Data Converters, Kluwer Publishers, 2005.
5	S. Kenneth S Kundert and Olaf Zinke, 'The Designers Guide to Verilog AMS; Kluwer Publications, 2004.
6	Jacob Baker, Harry W Li, and David E Boyce 'CMOS. Circuit Design Layout and Simulation'. Wiley- IEEE Press. 1998.

Category	Professional Elective			
Course code	192VL23B			
Course Title	**VLSI SIGNAL PROCESSING**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**REALIZATION OF DIGITAL FILTERS**	9
FIR Filter design -IIR filter design - Direct form I,II, Cascade, Parallel. Ladder Lattice filters.		
Unit-2	**ITERATION BOUND**	9
Introduction, Data flow graph representations, loop bound and iteration bound, Algorithms for computing Iteration bound, iteration Bound of multirate Data - Flow Graphs.		
Unit-3	**PIPELINING AND PARALLEL PROCESSING**	9
Introduction Pipelining of FIR Digital filters Parallel processing Pipelining and parallel processing for Low power.		
Unit-4	**TRANSFORMATIONS–RETIMING**	9
Introduction - Definitions and Properties Solving system of Inequalities Retiming Techniques. UNFOLDING: Introduction - An algorithm for unfolding - Properties of unfolding Critical path, unfolding and retiming -Application of unfolding. FOLDING: Introduction - folding Transformation Register Minimization Techniques - Register Minimization in folded Architectures		
Unit-5	**FAST CONVOLUTION**	9
Cook Toom algorithm -modified Cook - Toom algorithm Winogard algorithm- modified Winogard algorithm, Algorithmic strength reduction in filters and transforms-parallel FIR filters, Parallel architectures for Rank-order filter.		

References

1	John G Proakis and Dimitris G Manolakis, 'Digital signal processing - Principles. Algorithms and Applications Pearson. 2014.
2	Uwe Meyer Sane, "Digital Signal Processing with Field Programmable Gate Arrays', Springer, 2014.
3	Lonnie C Ludeman, 'Fundamentals of Digital Signal Processing', Wiley India (P) Ltd. 2010.
4	Peter Pirsch 'Architectures for Digital Signal Processing'. Wiley India (P) Ltd, 2009.
5	Keshab K Parhi. 'VLSI Digital Signal Processing Systems Design and Implementation', Wiley Inter science, 2007.

Category	Professional Elective			
Course code	192VL23C			
Course Title	**SEMICONDUCTOR MEMORY DESIGN AND TESTING**			
Semester –II	**Scheme and Credits**			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**RANDOM ACCESS MEMORY TECHNOLOGIES**	9

Static Random Access Memories (SRAM): SRAM cell structures. MOS SRAM Architecture. MOS SRAM cell and peripheral Circuit Operation. Bipolar SRAM Technologies, Silicon on insulator (S0I) Technology. Advanced SRAM Architectures and Technologies, Application Specific SRAMs. Dynamic Random Access Memories (DRAM): DRAM Technology Development CMOS DRAM, DRAM cell theory and advanced cell structures, BiCMOS DRAM, soft error failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM

Unit-2	**NON-VOLATILE MEMORIES:**	9

Masked Read only Memories (ROM), High Density ROMs, Programmable ROM, Bipolar ROMs, CMOS PROMS, Erasable(UV) Programmable ROM(EPROM), Floating, Gate EPROM Cell, One time Programmable EPROM (OTPEPROM), Electrically Erasable PROMS, EEPROM Technology and Architecture. Non volatile SRAM. Flash Memories (EPROM or EEPROM). Advanced Flash Memory Architecture, Content Addressable Memory.

Unit-3	**SEMICONDUCTOR MEMORY RELIABILITY**	9

General Reliability Issues-RAM Failure Modes and Mechanism Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification.

Unit-4	**SEMICONDUCTOR MEMORY RADIATION EFFECTS:**	9

Radiation Effects-Single Event Phenomenon (SEP)•Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures

Unit-5	**ADVANCED MEMORY TECHNOLOGIES:**	9

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories- Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D) -Memory Stacks and MCMs (3D).Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

References

1	Jesse Russell and Ronald Cohn, 'Content-Addressable Memory, Bookvika Publishing. 2012.
2	KiyooItoh, Masashi Horiguchi and Hitoshi Tanaka, 'Ultra-Low Voltage Nano-Scale Memories'. Springer. 2007.
3	Ashok K Sharma. 'Semiconductor Memories Technology, Testing and Reliability', Wiley, 2002.

4	Ashok K Sharma 'Advanced Semiconductor Memories - Architecture, Design and Applications, Wiley, 2002.
5	Betty Prince. 'Emerging Memories - Technologies and Trends, Kluwer Academic Publishers, 2002.

Category	Professional Elective			
Course code	192VL23D			
Course Title	**VLSI TECHNOLOGY**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**BASICS OF CRYSTAL GROWTH:**	9
Crystal structure- axes & planes. Crystal defects-Point defects & dislocations Crystal growth-Bridgman. Czochralski techniques & Zone process.		
Unit-2	**MATERIAL PROPERTIES**	9
Doping in the melt. Diffusion& ION Implantation: Nature of diffusion-interstitial Substitutional, interstitial substitutional movements, Diffusion constant, Dissociate process, Diffusion equation-D is constant & function. Diffusion systems, problems in Si Diffusion. Evaluation Techniques Ion Implantation: Penetration range, Implantation Damage. Annealing, Implantation Systems.		
Unit-3	**OXIDATION &EPITAXY OXIDATION**	9
Thermal Oxidation-Intrinsic, Extrinsic silicon Glass, Oxide formation, Kinetics of Oxide growth, Oxidation systems, Faults, Anodic Oxidation. EPITAXY: Vapor Phase Epitaxy (VPE)- transport, reaction and growth, Chemistry of growth. Insitu etching. Selective epitaxy. imperfections. Liquid Phase Epitaxy. LPE system, Evaluation of epitaxial layers.		
Unit-4	**ETCHING & UTHOGRAPNY: UTHOGRAPHY**	9
UthographyPattern generation & Masking, Printing & Engraving - Optical. E-Beam, ion Beam. X-Ray, Photo resists. Defects. ETCHING: Wet chemical etching- anisotropic etchants, Etching for noncrystalline lams-Plasma etching, Plasma-assisted etching, cleaning		
Unit-5	**DEVICE & CIRCUIT FABRICATION:**	9
Isolation- Mesa, Oxide, PN-junction isolations. Self Alignment. Local Oxidation, Planarization, Metallization and Packaging. Circuits - N, P and CMOS Transistors. Memory devices. BJT Circuits - Buried Layer. PNP and NPN Transistors, Diodes, Resistors, Capacitors.		

References

1	Donald Neamen, DhrubesBiswas, 'Semiconductor Physics and Devices' McGraw Hilt New York, Fourth edition, 2017.
2	Massimo Ruden , ;Physics of Semiconductor Devices, Springer, second edition.2017
3	Sze S M, 'VLSI Technology, McGraw Hill, New York. second edition, 2017.
4	Sorab K Gandhi, 'VLSI Fabrication Principles -Silicon and Gallium Arsenide'. Wiley Interscience Publications. New York 2008.
5	Chang S Y and Sze S M “ULSI Technology”. McGraw Hill, New York, 2007.
6	Sze S M and Kwok K Ng ;Physics of Semiconductor Devices, John Wiley, 2006.

Category	Professional Elective			
Course code	192VL23E			
Course Title	**VLSI FOR WIRELESS COMMUNICATION**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**OVERVIEW OF MODULATION SCHEMES**	9

Classical Channel - Wireless Channel Description - Path Loss - Channel Model and Envelope Fading Multipath Fading: Frequency Selective and Fast Fading - Summary of Standard Translation

Unit-2	**RECEIVER FRONT END**	9

Filter Design - Rest of Receiver Front End: Non-idealities and Design Parameters Nonlinearity - Noise-Derivation of Noise Figure. AMPLIFIER DESIGN: Low Noise Amplifier Design, Wideband LNA - Design Narrowband LNA -Impedance Matching - Automatic Gain Control Amplifiers - Power Amplifiers

Unit-3	**TYPES OF MIXERS**	9

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain - Distortion - Low Frequency Case: Analysis of Gilbert Mixer - Distortion - High-Frequency Case - Noise - A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer.

Unit-4	**NOISE IN MIXERS**	9

Conversion Gain in Unbalanced Switching Mixer Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer -Intrinsic Noise in Single Ended Sampling Mixer Extrinsic Noise in Single Ended Sampling Mixer- Demodulators

Unit-5	**FREQUENCY SYNTHESIZERS**	9

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector - Analog Phase Detectors - Digital Phase Detectors - Frequency Dividers - LC Oscillators -Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application). Loop filter:General Description - Design Approaches.

References

1	Luzzatto A and Shirazi G. 'Wireless Transceiver Design: Mastering the Design of Modern Wireless Equipment and Systems'. Wiley 2007.
2	Laskar*J*, Matinpourand B and Charaboty S. 'Modem receiver front ends:Systems, Circuits and integration", Wiley 2004
3	Bosco H Leung 'VLSI for Wireless Communications, Pearson Education, 2002
4	Leenearts D. Vander J Tang and Vaucher C S 'Circuit design for RF transceivers', Springer 2002.
5	S. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design Circuits and Systems. Kluwer Academic Publishers, 2000.

Category	Professional Elective			
Course code	192VL23F			
Course Title	**CPLD and FPGA Architecture and Applications**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**Introduction to Programmable Logic Devices**	9
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.		
Unit-2	**Field Programmable Gate Arrays**	9
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs		
Unit-3	**SRAM Programmable FPGAs**	9
Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures		
Unit-4	**Anti-Fuse Programmed FPGAs**	9
Introduction, Programming Technology, Device Architecture, the Actel ACT1, ACT2 and ACT3 Architectures.		
Unit-5	**Design Applications**	9
General Design Issues, Counter Examples, A Fast Video Controller, and A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.		

References

1	Stephen M. Trimberger, “Field Programmable Gate Array Technology”, Springer International Edition.
2	Charles H. Roth Jr, LizyKurian John, “Digital Systems Design”, Cengage Learning.
3	John V. Oldfield, Richard C. Dorf, “Field Programmable Gate Arrays”, Wiley India.
4	Pak K. Chan/SamihaMourad, “Digital Design Using Field Programmable Gate Arrays”, Pearson Low Price Edition.
5	Ian Grout, “Digital Systems Design with FPGAs and CPLDs”, Elsevier, Newnes.
6	Wayne Wolf, “FPGA based System Design”, Prentice Hall Modern Semiconductor Design Series.

Category	Professional Elective			
Course code	192VL23G			
Course Title	**SYSTEM ON CHIP DESIGN**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**LOGIC GATES**	9
Introduction. Combinational Logic Functions. Static Complementary Gates. Switch Logic. Alternative Gate Circuits. Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect. Objectives		
Unit-2	**COMBINATIONAL LOGIC NETWORKS**	9
Introduction. Standard Cell-Based Layout. Simulation. Combinational Network Delay. Logic and interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.		
Unit-3	**SEQUENTIAL MACHINES**	9
Introduction. Latches and Flip-Flops. Sequential Systems and Clocking Disciplines. Sequential System Design. Power Optimization. Design Validation. Sequential Testing.		
Unit-4	**SUB SYSTEM DESIGN**	9
Introduction. Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers. High-Density Memory. Field Programmable Gate Arrays. Programmable Logic Arrays. References. Problems.		
Unit-5	**FLOOR-PLANNING**	9
Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections – Packages, The I/O Architecture, PAD Design.		

References

1	Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition, 2008
2	Wayne Wolf , “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition, 2008.

Category	Professional Elective			
Course code	192VL23H			
Course Title	**MEMS AND NEMS**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**INTRODUCTION AND SCALING**	9

MEMS and Microsystems development of MEMS technology- MEMS future and applications, Microsystems and microelectronics MEMS challenges - scaling - scaling in geometry, rigid body dynamics, electrostatic forces, electromagnetic forces, electricity, fluid mechanics, heat transfer.

Unit-2	**MATERIALS FOR MEMS:**	9

Introduction - substrates and wafer silicon substrate crystal structure, miller indices, properties silicon compounds silicon dioxide, silicon carbide, silicon nitride, polycrystalline silicon- gallium arsenide - quartz- piezoelectric crystals -polymers polymers for MEMS, conductive polymers.

Unit-3	**FABRICATION PROCESS:**	9

Physical Vapour Deposition (PVD) evaporation, sputtering Chemical Vapour Deposition (CVD) etching process wet chemical etching, plasma etching. Ion milling patterning - lithography, lift off process wafer bonding - silicon fusion bonding, anodic bonding- annealing- chemical mechanical polishing - doping - diffusion, implant.

Unit-4	**MEMS TECHNOLOGIES AND PACKAGING:**	9

Bulk micromachining Isotropic and anisotropic etching. wet etchants. etch stop, dry etching, comparison of wet and dry etching surface micromachining Introduction, process, associated problems LICA Process and electroplating - Integration of electronics and MEMS technology- packaging post fabrication process, package selection, die attach. Wire bond and Sealing.

Unit-5	**HEMS TECHNIQUES AND APPLICATIONS:**	9

Introduction to NEMS and its architecture carbon nanotube electronics modeling -introduction, analysis and simulation - simulation of Actuators, FET, Pressure transducer applications and future challenges.

References

1	Ananthasuresh G. K, Vinoy. K.J, Gopalakristman.S, 'Micro and Smart Systems, Wiley India PA Ltd, New Delhi, 2012.
2	Vijay K. Varadan, Vinoy. KJ, Gopalakrishnan.S. "Smart material Systems and MEMS: Design and Development Methodologies, John Wiley & Sons, New York. 2011.
3	Tai Ran Hsu. 'MEMS and Microsystems. Design. Manufacture and Nanoscale Engineering. John Wiley & Sons, New Jersey. 2008.
4	James J Allen, "Micro Electro Mechanical System Design CRC Press-Taylor & Francis', New Yolk 2005.
5	Sergey Edward Lyshevski. 'MEMS and NEMS systems, Devices and Structures'. CRC Press. New York. 2002.

Category	Professional Elective			
Course code	192VL23I			
Course Title	**EMBEDDED SYSTEM DESIGN**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**EMBEDDED DESIGN CYCLE OVERVIEW:**	9

Differences between the Desktop PC and typical Embedded SystemExamples of Embedded Systems-Major hardware and software modules of an embedded system-Embedded Design Life Cycle. Introduction to ARM Controllers:ARMCortex-A. Cortex-R and Cortex-M series microcontrollers

Unit-2	**INTRODUCTION TO PERIPHERALS**	9

CPU Core, Program Memory. Data Memory, AHP and APB Bus Structure. System Peripherals: GPIO, Timers, EEPROM, Hibernation Module, WDT and DMA. Serial Peripherals: UART, I^2C, SPI, CAN and USB.

Unit-3	**PERIPHERAL INTERFACING TECHNIQUES:**	9

Analog Peripherals: ADC and Analog Comparator. Motion Control Peripherals: PWM and QEI Hardware and Software Interrupts, Clock and Reset Generator. Development and debugging Support :JTAG and BDM.

Unit-4	**PERIPHERAL PROGRAMMING TECHNIQUES:**	9

Host and Target Machines. Configuring and Programming of System Peripherals, Serial Peripherals, Analog Peripherals and Motion Control Peripherals. Display, Keyboard, Sensors, motors, interfacing and Programming Techniques.

Unit-5	**REAL TIME OPERATING SYSTEMS (RTOS)**	9

Survey of software architectures. Tasks and Task States, Tasks and Data. Semaphores and Shared Data, Message Queues, Mailboxes and Pipes, Timer functions, Events, Memory Management, Interrupt Routines in RTOS Environment.

References

1	Steve Furber, ARM System-on-Chip Architecture. Prentice Hall of India. New Delhi. 2009.
2	David E Simon, "An Embedded Software Primer" Pearson Education Asia. 2006.
3	Arnold S. Berger, 'Embedded Systems Design:An Introduction to Processes, Tools, and Techniques" CMP Books. 2002.
4	https:/www.arm.com/products/processors
5	https:/www.ti.com/tiva
6	https:/www. nordicsemi.com/eng/Products/Nordic-Thingy-52

Category	Professional Elective			
Course code	192VL23J			
Course Title	**ANALOG TO DIGITAL INTERFACES**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**SAMPLE AND HOLD CIRCUITS**	9
Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture		
Unit-2	**SWITCHED CAPACITOR CIRCUITS AND COMPARATORS**	9
Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.		
Unit-3	**DIGITAL TO ANALOG CONVERSION**	9
Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.		
Unit-4	**ANALOG TO DIGITAL CONVERSION**	9
Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture		
Unit-5	**PRECISION TECHNIQUES**	9
Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.		

References

1	BehzadRazavi, “Principles of data conversion system design”, S. Chand and company Ltd, 2000.

PROFESSIONAL ELECTIVE THEORY COURSES (Three to be opted for third semester)

Category	Professional Elective			
Course code	192VL33A			
Course Title	**HIGH SPEED DIGITAL DESIGN**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**TRANSMISSION LINES AND CROSSTALK**	9
Transmission line structures, signal propagation, transmission line parameters, line impedance, Propagation delay. Transmission line reflections, Cross talk- Mutual inductance, Mutual capacitance, cross talk induced noise, minimizing cross talk		
Unit-2	**INTERCONNECTS**	8
Interconnect technologies, Multilevel multilayer, interconnects, propagation delay. crosstalk analysis		
Unit-3	**POWER and CLOCK DISTRIBUTION**	10
Losses, the need for low-impedance planes and decoupling capacitors and their selection High-quality clock signals to components, boards, and systems, Common clock timing and source synchronous timing		
Unit-4	**ELECTROMAGNETIC COMPATIBILITY (EMC)**	9
Designing for EMC, EMC regulations, typical noise path, methods of noise coupling, and methods of reducing interference in systems.		
Unit-5	**GROUNDING**	9
Safety grounds, signal grounds, single-point ground systems, multi-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies.		

References

1	Goel A K, "High speed VLSI interconnections' Wiley, 2007.)
2	Paul CR:Introduction to Electromagnetic compatibility, Wiley 2006.
3	Howard Johnson, Martin Graham. 'High speed Digital design. Pearson. 2005.
4	Bogatin E, 'Signal integrity -simplified', Prentice Hall, 2003.
5	Hall S . Hall G and McCall J, " High speed digital system design: AHandbook of Interconnect theory and practices, Wiley Interscience, 2000
6	Hartman Grabinski. ‘Interconnects in VLSI design'. Kluwer, 2000.

Category	Professional Elective			
Course code	192VL33B			
Course Title	**NANO SCALE DEVICES**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**OVERVIEW**	9

Nano devices. Nano materials. Nano characterization-Definition of Technology node. Basic CMOS Process flow- MOS Scaling theory, Issues in scaling. MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology-- Requirements for Non-classical MOS transistor.

Unit-2	**MOS CAPACITOR**	9

Role of interface quality and related process techniques, Gate oxide thickness scaling trend, Si02 vs. High-k gate dielectrics- Integration issues of high-k -Interface states, bulk charge, band offset. stability, reliability Qs, high field. Possible candidates. CV and IV techniques.

Unit-3	**METAL GATE TRANSISTOR**	9

Motivation, requirements, Integration Issues Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot Ultrathin body 501 double gate transistors, integration issues - Vertical transistors - FinFET and Surround gate FET.

Unit-4	**METAL SOURCE/DRAIN JUNCTIONS:**	9

Properties of schotky junctions on Silicon, Germanium and compound semiconductors -Work function pinning- Germanium Nano MOSFETs: strain, quantization. Advantages of Germanium over Silicon. PMOS versus NMOS. Compound semiconductors material properties. MESFETs Compound semiconductors MOSFETs in the context of channel quantization and strain. Hetero structure MOSFETs exploiting novel materials, strain, and quantization.

Unit-5	**SYNTHESIS OF NANOMATERIALS**	9

CVD, Nucleation and Growth, ALD, Epitaxy, MBE. Compound semiconductor hetero-structure growth and characterization Quantum wells and Thickness measurement techniques -Contact - step height. Optical - reflectance and ellipsometry.AEM. Characterization techniques for nanomaterials: FTIR. XRD, AFM. SEM, TEM, EDAX etc-Applications and interpretation of results. EMERGING NANO MATERIALS: Nanotubes, nanorods and other Nano structures. LB technique. Soft lithography. Microwave assisted synthesis. Self assembly.

References

1	Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices. Springer. 2005.
2	WaserRanier."Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices, Wiley-VCH, 2005.

Category	Professional Elective			
Course code	192VL33C			
Course Title	**MODELING AND SIMULATION OF NANOSCALE TRANSISTORS**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**ANALYTICAL MODELLING**	9
Introduction - Types of Models - Attributes of Good Compact Models - Model Formulation - Model Implementation in Circuit Simulators Model Testing - Parameter Extraction - Simulation and Extraction for RF Applications. Analytical Solution Methods: Parabolic Approximation Variable Separable Numerical Simulation Fourier series - Green Function -Bessel Function.		
Unit-2	**TECHNOLOGY-ORIENTED CAD & DEVICE CAD**	9
Introduction - Process and Device CAD - Process Simulation Techniques -Interfaces in process and Device CAD - CMOS Technology - Ion Implantation - Oxidation - Impurity Diffusion.		
Unit-3	**DEVICE CAD**	9
Semiconductor Device Analysis - The PN Junction - Equilibrium Conditions - Non-equilibrium Conditions - Bipolar Junction Structures Carrier Densities - Carrier Transport and Conversation - Field-Effect Structures. The MOS capacitor - Basic MOSFET I-V Characteristics - Threshold Voltage in Nonuniform Substrate - MOS device Design by Simulation.		
Unit-4	**TCAD SIMULATION**	9
Process simulator - Device simulator - Advanced concepts - drift-diffusion, hydrodynamic model, stress models Structure editor meshing concepts - work bench - Plotting - Scripting -Monte-carlo simulation Electromagnetic simulation.		
Unit-5	**NOVEL TRANSISTOR ARCHFIECTURES**	9
Nanowire transistor - High electron mobility transistor Tunnel field effect transistor - Single electron transistor - Carbon nanotube transistor - Double gate and multi gate MOS transistor - Electron wave transistor Electron spin transistor.		

References

1	Robert W.Dutton and Zhiping Yu, 'Technology CAD Computer Simulation of Processes and Devices. Springer, 2012.
2	Rainer Waser. 'Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices'. 3rd Edition. Wiley VchVerlag, Weinheim, 2012.
3	YannisTsividis and Colin McAndrew, 'Operation and Modeling of the MOS Transistor, 3rd Edition, Oxford University Press, 2011
4	Mark S. Lundstrom and Jing Guo, 'NanoscaleTransistors:Device Physics. Modeling and Simulation, Springer. 2006
5	ShunriOda and David Ferry,'SiliconNanoelectronicst CRC Press, New York, 2005.
6	Karl Golser, Peter Glosekotter and Jan Dienstuhl, ¯Nanoelectronics and Nanosystems Springer. 2004.

Category	Professional Elective			
Course code	192VL33D			
Course Title	**ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**INTRODUCTION TO PARALLELPROCESSING**	9

Evolutionofcomputersystems. Generationofcomputer systems TrendstowardsparallelprocessingParallelprocessing mechanisms parallel Computer structure Architectural classificationschemes Application

Unit-2	**MEMORY AND I/O SUBSYSTEMS, PIPELENING**	9

Hierarchical Memory structure - Virtual memory system - cache memory management- Memory allocation and management - I/O subsystems pipelining: Principles - Classification of pipeline processors -Reservation tables - Interleaved memory organization - Design of arithmetic pipeline - Design of instruction pipeline.

Unit-3	**VECTOR AND ARRAY PROCESSING**	9

Need - Basic vector processing architecture - Issues in vector processing - Vectorization and optimization methods. Array processing: SIMD Array processors - SIMD interconnection networks - Parallel algorithms for array processors - associative array processing

Unit-4	**MULTIPROCESSOR ARCHITECTURE**	9

Functional structures - Interconnection network - Multi cache problems and solutions -Exploiting concurrency for multiprocessing

Unit-5	**PRINCIPLES OF PARALLEL ALGORITHM DESIGN**	9

Design approaches-Design issues-Performance measures and analysis-Complexities-Anomalies in parallel algorithms - Pseudo code conventions for parallel algorithms-Comparison of SIMD and MIMD algorithms.

References

1	Kai Hwang, NareshJotwani: Advanced Computer Architecture - Parallelism, Scalability, Programmability, Tata McGraw Hill, 2011
2	John L Hennessy, "Computer Architecture a Quantitative Approach", Harcourt Asia Pvt. Ltd., 2011.
3	SeyedRoosta, Parallel Processing and Parallel Algorithms", Springer Series, 2000.

Category	Professional Elective			
Course code	192VL33E			
Course Title	**ADVANCED DIGITAL IMAGE PROCESSING**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**FUNDAMENTALS OF DIGITAL IMAGEPROCESSING**	9

Elements of image perception, Brightness, Contrast, Hue, Saturation, Match Band Effect, 2D image transforms-DFT,DCT, KLT and SVD

Unit-2	**IMAGE ENHANCEMENT**	9

Spatial Filters: Point processing, Some Basic Gray Level Transformations, Histogram Processing, Enhancement Using Arithmetic/Logic Operations, Basics of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
Frequency Domain Filters: Smoothing Frequency-Domain Filters , Sharpening Frequency Domain Filters, Homomorphic Filtering

Unit-3	**IMAGE SEGMENTATION**	9

Edge Linking and Boundary Detection, Thresholding, Basic Formulation, Region Growing, Region Splitting and Merging, Dam Construction, Watershed Segmentation Algorithm, Segmentation in HSI Color Space, Segmentation in RGB Vector Space, Color Edge Detection

Unit-4	**IMAGE RESTORATION AND COLOR IMAGE PROCESSING**	9

Image Degradation/Restoration Process, Noise Models, Mean Filters, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering, Color Fundamentals, Color Models, Pseudocolor Image Processing, Smoothing and Sharpening, Color Segmentation

Unit-5	**IMAGE COMPRESSION AND REPRESENTATION**	9

Coding Redundancy, Interpixel Redundancy, Psychovisual Redundancy, Fidelity Criteria , The Source Encoder and Decoder, The Channel Encoder and Decoder, Measuring Information, The Information Channel, Fundamental Coding Theorems, Using Information Theory, Representation, Boundary Descriptors, Regional Descriptors, Recognition Based on Decision-Theoretic Methods

References

1	Gonzalez and Woods, Digital Image Processing, Prentice-Hall.
2	A.K. Jain, “Fundamentals of Digital Image Processing”, Prentice-Hall, Addison-Wesley, 1989.
3	J. C. Russ. The Image Processing Handbook. CRC, Boca Raton, FL, 4th edn., 2002.
4	W. K. Pratt. Digital image processing, PIKS Inside. Wiley, New York, 3rd, edn., 2001.

Category	Professional Elective			
Course code	192VL33F			
Course Title	**SELECTED TOPICS IN IC DESIGN**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**VOLTAGE AND CURRENT REFERENCES**	9
Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing		
Unit-2	**LOW DROP OUT REGULATORS**	9
General layout and construction consideration ,Output Voltage Accuracy, Design issues and general applications		
Unit-3	**OSCILLATOR FUNDAMENTALS**	9
General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC Oscillators.		
Unit-4	**PHASE LOCK LOOPS**	9
PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance.		
Unit-5	**CLOCK AND DATA RECOVERY**	9
CDR Architectures, Tias and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.		

References

1	BehzadRazavi, “Design of Integrated circuits for Optical Communications”, McGraw Hill, 2003.
2	Floyd M. Gardner ,”Phase Lock Techniques” John wiley& Sons, Inc 2005.
3	Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgapcircuits”,Johnwiley& Sons, Inc 2002.
4	MichielSteyaert, MichielSteyaert, Arthur H.M. van Roermund, Herman Casier “Analog Circuit Design - High Speed Clock and Data Recovery, High-performance Amplifiers Power Management “ springer, 2008.

Category	Professional Elective			
Course code	192VL33G			
Course Title	**ELECTRONIC PACKAGING TECHNOLOGIES**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**OVERVIEW OF ELECTRONIC SYSTEMS PACKAGING:**	9
Packaged Electronics - Technologies- Trends- Products and levels of packaging- Packaging aspects of handheld products.		
Unit-2	**BASICS OF SEMICONDUCTOR PACKAGING:**	9
Basics of Semiconductor and Process flowchart; Wafer packaging; Packaging evolution- Chip connection choices -Wire bonding, TAB and flip chip. Single chip packages or modules (SCM).		
Unit-3	**TYPES OF PACKAGING**	9
Commonly used packages and advanced packages; Materials in packages- Advances packages Thermal mismatch in packages; Current trends in packaging-Multichip modules (MCM)-types; System-in package(SIP)- Packaging roadmaps- Hybrid circuits.		
Unit-4	**ELECTRICAL DESIGN CONSIDERATIONS IN SYSTEMS PACKAGING:**	9
Electrical Issues - Resistive Parasitic - Capacitive and Inductive Parasitic- Layout guidelines and the Reflection problem-Interconnection.		
Unit-5	**THERMAL MANAGEMENT AND RELIABILITY:**	9
Heat-transfer fundamentals-. Thermal conductivity and resistance- Conduction, convection and radiation- Cooling -Reliability- Basic concepts- Environmental interactions- Thermal mismatch and fatigue.		

References

1	Rao R Tummala, "Fundamentals of Microsystems Packaging", McGraw Hill, NY, 2001
2	William D Brown, "Advanced Electronic Packaging", IEEE Press, 1999

Category	Professional Elective			
Course code	192VL33H			
Course Title	**VLSI FOR IoT SYSTEMS**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**INTRODUCTION**	9

Concept of connected world - Need, Legacy systems for connected world - features and limitations, Key features of loT architecture, Merits and Demerits of loT technology, Applications driven by loT technology - examples

Unit-2	**COMPONENTS OF IoT**	9

Review of classic embedded system architecture, Basic building blocks of anloT system - Artificial Intelligence, Connectivity, Sensors and Computing nodes. Sensors used in loT systems - Characteristics and requirements, Types of sensors for loT systems, Compute nodes of loT, Connectivity technologies in loT - Software in loT systems - features and properties.

Unit-3	**IC TECHNOLOGY FOR IoT**	9

SoC architecture for loT Devices - Application Processors, Microcontrollers, Smart Analog; Memory architecture for loT - Non Volatile Memories (NVM), Embedded Non-Volatile Memories, Anti-Fuse One Time Programmable (OTP) memories, Power Management - Low Drop Out Regulators, DC-to-DC Converters, Voltage References, Power Management Units (PMUs) in IC's and Systems, Role of Field Programmability in loT systems.

Unit-4	**ELECTRONIC SYSTEM DESIGN FOR IoT**	9

Electronic System Design for loT - Requirements, Computing blocks in loT systems - MCU's, DSPs and FPGA's, System Power Supply Design for loT systems, Mixed Signal challenges in hardware systems, Form Factor - Guidelines and prevailing standards.

Unit-5	**ELECTRONIC SYSTEM DESIGN CHALLANGES**	9

Component models & System Design - Feasibility and challenges, System Level Integration, Operating conditions of loT devices and impact on Electronic System Design; Hardware Security issues, EMI/EMC, SI/PI and Reliability Analysis in loT systems.

References

1	Alloto, "Enabling the Internet of Things- From Integrated Circuits to Integrated Systems", Springer Publications, First Edition, 2017.
2	Pieter Harpe, Kofi A. A. Makinwa, Andrea Baschirotto, "Hybrid ADCs, Smart Sensors for the loT, and Sub-1V & Advanced Node Analog Circuit Design", Springer International Publishing AG, 2017
3	Rashid Khan, KajariGhoshdastidar, AjithVasudevan, "Learning loT with Particle Photon and Electron", Packt Publishing Limited (Verlag), 2016.
4	ApekMulay, "Sustaining Moore's Law: Uncertainty Leading to a Certainty of loT Revolution" Morgan and Claypool Publishers, 2015.
5	OrCAD, "P-spice Technology for Internet of Things" - https:/www.pspice.com/solution/pspice-technology-internet-things
6	Jim Lipman, Sidense Corp." NVM memory: A Critical Design Consideration for loT Applications"- https:/www.design-reuse.com/articles/32614/nvm-memory-iot-applications.html

Category	Professional Elective			
Course code	192VL33I			
Course Title	**Quantum Dot Cellular Automata Nano Technology**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**INTRODUCTION**	9

Emerging Nanotechnologies- Electronics beyond Moore's law - Limitations of CMOS technology- Alternatives to MOSFET and Challenges - Emerging Transistor Based Devices-IC Technology beyond CMOS Era- USDM and Quantum computing-QCA modeling approach.

Unit-2	**QCA TERMINOLOGY**	9

QCA Basics - Schrodinger's equation in quantum wires - Quantum boxes - Non-zero angular momentum states- Spherical quantum dots -Tiny quantum dots- Cuboidal dots- Dots of arbitrary shape -Approaches to pyramidal dots- Matrix approaches-Transport through dot arrays- Crossovers in QCA -Convergence tests- Efficiency- Tool for QCA Simulation.

Unit-3	**BASIC COMPONENTS IN QCA**	9

Logic Primitives in QCA- Clocking in QCA - Role and Types -Design of Logic Gates and Multiplexer in QCA - Design of a One-Bit Full-Adder - Flip-Flop in QCA. Adders and Multipliers In QCA

Unit-4	**DESIGN OF DIGITAL CIRCUITS IN QCA**	9

Design of Ripple Carry Adder (RCA) and Prefix Adders in QCA- Design of 16-Bit Hybrid Adder in QCA- Layout Level Implementation of adders and Comparisons. Introduction to Multipliers - Design of a Multiplier in QCA - The Baugh - Wooley Multiplier for 2's Complement Numbers- Design of Baugh-Wooley Multiplier in QCA.

Unit-5	**TRANSFORM IN QCA**	9

Discrete Hadamard Transform Computation in QCA - Basics of Discrete Hadamard Transform- Mathematical Formulation for DHT Computation- QCA Realization - Performance of a Full-Parallel Addition Strategy - Applications of Quantum Dot Cellular Automata Technology.

References

1	Paul Harrison, Alex Valavanis -Quantum Wells, Wires and Dots: Theoretical and Computational Physics of Semiconductor Nanostructures, 4th Edition, Wiley, April 2016.
2	K. Sridharan, VikramkumarPudi -Design of Arithmetic Circuits in Quantum Dot Cellular Automata Nanotechnology Studies in Computational Intelligence-Springer International Publishing-2015.
3	Fabrizio Lombardi, Jing Huang - Design and Test of Digital Circuits by Quantum-Dot Cellular Automata-Artech House-2007.
4	Kasper, E., Paul, D -Silicon Quantum Integrated Circuits -Silicon-Germanium Heterostructure Devices: Basics and Realisations-Springer-Verlag Berlin Heidelberg 2005.
5	Paul Harrison, Alex Valavanis -Quantum Wells, Wires and Dots: Theoretical and Computational Physics of Semiconductor Nanostructures, 4th Edition, Wiley, April 2016.
6	K. Sridharan, VikramkumarPudi -Design of Arithmetic Circuits in Quantum Dot Cellular Automata Nanotechnology Studies in Computational Intelligence-Springer International Publishing-2015.

Category	Professional Elective			
Course code	192VL33J			
Course Title	**Genetic Algorithms for VLSI Design**			
	Scheme and Credits			
	L	**T**	**P**	**Credits**
	3	0	0	3

Unit-1	**GA OPERATORS AND GA FORALGORITHM**	9
Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion		
Unit-2		9
GA for VLSI Design, Layout and Test automation-partitioning- automatic placement, routing technology, Mapping for FPGA -Automatic test generation-Partitioning algorithm Taxonomy - Multiway Partitioning		
Unit-3	**GA FOR PARTITIONING,PLACEMENT AND ROUTING**	9
Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.		
Unit-4	**AUTOMATIC TEST GENERATION**	9
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.		
Unit-5	**PEAK POWER ESTIMATION AND PARALLEL IMPLEMENTATIONS**	9
Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.		

References

1	PinakiMazumder, E MRudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall, 1998
2	Randy L Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms", Wiley-Interscience,2004.
3	Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B R Vellasco and Marley Maria Bernard Vellasco, "Evolution Electronics:Automatic Design of Electronic Circuits and Systems Genetic Algorithms", CRC press, 2001
4	John R Koza, Forrest H Bennett ID, David Andre and Morgan Kufmann, "Genetic Automatic Programming and Circuit Synthesis", 1999